

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	77	703/14.ccls. and @pd>"20050601"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 14:56
L5	57	(715/771.CCLS. or 715/762.CCLS.) and @pd>"20050601"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:22
L6	3602	(fifo or tri-state) and simulation	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:24
L9	2537	L6 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:30
L10	1990	L9 and fifo	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:31
L11	751	L9 and tri-state	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:32
L12	106	L10 and simulat\$5.ti.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:40
L13	58	L11 and simulat\$5.ti.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:44
L15	303	L9 and (verilog or vhdl)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/31 15:45


 [Search Results](#)
[BROWSE](#)[SEARCH](#)[IEEE Xplore Guide](#)

Results for "((fifo<and>simulation)<and>verilog) <and> (pyr >= 1951 <and> pyr <= 20..."

[e-mail](#)

Your search matched 81 of 1253851 documents.

A maximum of 250 results are displayed, 50 to a page, sorted by **Relevance** in **Descending** order.» [Search Options](#)[View Session History](#)[New Search](#)[Modify Search](#)

[»](#)
 Check to search only within this results set
Display Format: Citation Citation & Abstract» [Key](#)
 [Select](#) [Article Information](#)

IEEE JNL IEEE Journal or Magazine

- 1. **A 2.5 Gb/s ATM switch chip set**
Plaza, P.; Merayo, L.A.; Diaz, J.C.; Conesa, J.L.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 4, Issue 3, Sept. 1996 Page(s):405 - 416
Digital Object Identifier 10.1109/92.532040
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1752 KB\)](#) IEEE JNL

IEEE JNL IEEE Journal or Magazine

- 2. **Design of embedded systems: formal models, validation, and synthesis**
Edwards, S.; Lavagno, L.; Lee, E.A.; Sangiovanni-Vincentelli, A.;
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):366 - 390
Digital Object Identifier 10.1109/5.558710
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(252 KB\)](#) IEEE JNL

IEEE CNF IEEE Conference Proceeding

- 3. **Core design and system-on-a-chip integration**
Rincon, A.M.; Cherichetti, G.; Monzel, J.A.; Stauffer, D.R.; Trick, M.T.;
Design & Test of Computers, IEEE
Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):26 - 35
Digital Object Identifier 10.1109/54.632878
[AbstractPlus](#) | [Full Text: PDF\(228 KB\)](#) IEEE JNL

IEEE CNF IEEE Conference Proceeding

- 4. **Scalable hardware priority queue architectures for high-speed packet switching**
Sung-Whan Moon; Rexford, J.; Shin, K.G.;
Computers, IEEE Transactions on
Volume 49, Issue 11, Nov. 2000 Page(s):1215 - 1227
Digital Object Identifier 10.1109/12.895938
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(376 KB\)](#) IEEE JNL

IEEE STD IEEE Standard

- 5. **Design and modelling of a high performance differential bipolar self-timed microprocessor**
Kelly, R.; Brackenbury, L.E.M.;
Computers and Digital Techniques, IEE Proceedings-
Volume 144, Issue 6, Nov. 1997 Page(s):371 - 380
[AbstractPlus](#) | [Full Text: PDF\(992 KB\)](#) IEE JNL

- 6. **IEEE standard Verilog hardware description language**
IEEE Std 1364-2001
2001 Page(s):0_1 - 856
[AbstractPlus](#) | [Full Text: PDF\(3773 KB\)](#) IEEE STD

- 7. **ATM traffic shaper: ATS**
Diaz, J.C.; Plaza, P.; Crespo, J.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):96 - 101
Digital Object Identifier 10.1109/DATE.1998.655842
[AbstractPlus](#) | Full Text: [PDF\(400 KB\)](#) IEEE CNF

- 8. **An example of a digital synthesis approach to DSP design: the AGS Transistor**
Brown, K.A.; Smith, G.; Wong, V.;
Particle Accelerator Conference, 1997. Proceedings of the 1997
Volume 2, 12-16 May 1997 Page(s):2302 - 2304 vol.2
Digital Object Identifier 10.1109/PAC.1997.751189
[AbstractPlus](#) | Full Text: [PDF\(196 KB\)](#) IEEE CNF

- 9. **High-density zero suppressor and encoder VME board using field programmable array**
Aloisio, A.; Cevenini, F.; Patricelli, S.; Parascandolo, P.;
Nuclear Science, IEEE Transactions on
Volume 41, Issue 1, Part 1-2, Feb 1994 Page(s):225 - 227
Digital Object Identifier 10.1109/23.281494
[AbstractPlus](#) | Full Text: [PDF\(180 KB\)](#) IEEE JNL

- 10. **Data scanner and event builder for the SMVD of the KEK B-factory**
Tanaka, M.; Ikeda, H.; Ikeda, M.; Fujita, Y.; Ozaki, H.; Fukunaga, C.;
Nuclear Science, IEEE Transactions on
Volume 41, Issue 1, Part 1-2, Feb 1994 Page(s):252 - 256
Digital Object Identifier 10.1109/23.281500
[AbstractPlus](#) | Full Text: [PDF\(384 KB\)](#) IEEE JNL

- 11. **The module controller chip (MCC) of the ATLAS pixel detector**
Beccherle, R.;
Nuclear Science Symposium, 1998. Conference Record. 1998 IEEE
Volume 1, 8-14 Nov. 1998 Page(s):69 - 74 vol.1
Digital Object Identifier 10.1109/NSSMIC.1998.774811
[AbstractPlus](#) | Full Text: [PDF\(576 KB\)](#) IEEE CNF

- 12. **A 16-channel digital TDC chip**
Bailly, P.; Chauveau, J.; Genat, J.F.; Huppert, J.F.; Lebbolo, H.; Roos, L.; Zhai, Y.;
Nuclear Science Symposium, 1998. Conference Record. 1998 IEEE
Volume 1, 8-14 Nov. 1998 Page(s):447 - 452 vol.1
Digital Object Identifier 10.1109/NSSMIC.1998.775181
[AbstractPlus](#) | Full Text: [PDF\(352 KB\)](#) IEEE CNF

- 13. **The START-VOYAGER parallel system**
Ang, B.S.; Chiou, D.; Rudolph, L.; Arvind;
Parallel Architectures and Compilation Techniques, 1998. Proceedings. 1998 International Conference on
12-18 Oct. 1998 Page(s):185 - 194
Digital Object Identifier 10.1109/PACT.1998.727191
[AbstractPlus](#) | Full Text: [PDF\(152 KB\)](#) IEEE CNF

- 14. **A prototype data acquisition system for the BELLE vertex detector**
Nobori, T.; Uchida, T.; Fukunaga, C.; Tanaka, M.; Ikeda, H.;
Nuclear Science, IEEE Transactions on
Volume 43, Issue 3, Part 2, June 1996 Page(s):1795 - 1798
Digital Object Identifier 10.1109/23.507224
[AbstractPlus](#) | Full Text: [PDF\(340 KB\)](#) IEEE JNL

- 15. **Using term rewriting systems to design and verify processors**
Arvind; Shen, X.;
Micro, IEEE
Volume 19, Issue 3, May-June 1999 Page(s):36 - 46

Digital Object Identifier 10.1109/40.768501

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(2052 KB) IEEE JNL

- **16. An all-digital low-power IF GPS synchronizer**
Won Namgoong; Reader, S.; Meng, T.H.;
Solid-State Circuits, IEEE Journal of
Volume 35, Issue 6, June 2000 Page(s):856 - 864
Digital Object Identifier 10.1109/4.845189
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(688 KB) IEEE JNL
- **17. OMI-compliant model for virtual emulation**
Dozza, D.; Rambaldi, R.; Borgatti, M.; Guerrieri, R.;
Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Works
3-5 June 1998 Page(s):64 - 69
Digital Object Identifier 10.1109/IWRSP.1998.676670
[AbstractPlus](#) | Full Text: [PDF](#)(148 KB) IEEE CNF
- **18. Analysis and synthesis of concurrent digital circuits using control-flow e**
Coelho, C.N., Jr.; De Micheli, G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 15, Issue 8, Aug. 1996 Page(s):854 - 876
Digital Object Identifier 10.1109/43.511567
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(2248 KB) IEEE JNL
- **19. Program implementation schemes for hardware-software systems**
Gupta, R.K.; Claudio, N.C., Jr.; De Micheli, G.;
Computer
Volume 27, Issue 1, Jan. 1994 Page(s):48 - 55
Digital Object Identifier 10.1109/2.248880
[AbstractPlus](#) | Full Text: [PDF](#)(1188 KB) IEEE JNL
- **20. Simulating Multimedia Systems with MVPSIM**
Jihong Kim; Yongmin Kim;
Design & Test of Computers, IEEE
Volume 12, Issue 4, Winter 1995 Page(s):18
Digital Object Identifier 10.1109/MDT.1995.473309
[AbstractPlus](#) | Full Text: [PDF](#)(816 KB) IEEE JNL
- **21. Ravel-XL: a hardware accelerator for assigned-delay compiled-code logic**
Ripe, M.A.; Silva, J.P.M.; Sakallah, K.A.; Brown, R.B.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 4, Issue 1, March 1996 Page(s):113 - 129
Digital Object Identifier 10.1109/92.486085
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1884 KB) IEEE JNL
- **22. Designing electronic engines with electronic engines: 40 years of bootstrap technology upon itself**
Jess, J.A.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1404 - 1427
Digital Object Identifier 10.1109/43.898824
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(280 KB) IEEE JNL
- **23. An operational framework for the multi-lingual system simulation based on Chilean**
Windisch, A.; Monjau, D.;
Computer Science Society, 2001. SCCC 2001. Proceedings. XXI International Conference on Chilean
7-9 Nov. 2001 Page(s):282 - 291
Digital Object Identifier 10.1109/SCCC.2001.972658
[AbstractPlus](#) | Full Text: [PDF](#)(1585 KB) IEEE CNF

□ 24. **Top-down design using cycle based simulation: an MPEG A/V decoder** e;
Hocevar, D.E.; Ching-Yu Hung; Pickens, D.; Sriram, S.;
VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on
19-21 Feb. 1998 Page(s):400 - 405
Digital Object Identifier 10.1109/GLSV.1998.665333
[AbstractPlus](#) | Full Text: [PDF\(40 KB\)](#) IEEE CNF

□ 25. **On the way to the 2.5 Gbits/s ATM network ATM multiplexer demultiplexer**
Riesco, J.; Diaz, J.C.; Merayo, L.A.; Conesa, J.L.; Santos, C.; Juarez, E.;
European Design and Test Conference, 1997. ED&TC 97. Proceedings
17-20 March 1997 Page(s):218 - 222
Digital Object Identifier 10.1109/EDTC.1997.582362
[AbstractPlus](#) | Full Text: [PDF\(376 KB\)](#) IEEE CNF

□ 26. **Simulation of a macro-pipelined multi-CPU event processor for use in FA**
Letheren, M.F.; Marchioro, A.; Slorach, F.;
Nuclear Science, IEEE Transactions on
Volume 36, Issue 5, Oct 1989 Page(s):1597 - 1601
Digital Object Identifier 10.1109/23.41111
[AbstractPlus](#) | Full Text: [PDF\(468 KB\)](#) IEEE JNL

□ 27. **A proposed scalable parallel open architecture data acquisition system for future particle experiments, test beams and all SSC detectors**
Barsotti, E.; Booth, A.; Bowden, M.; Swoboda, C.; Lockyer, N.; VanBerg, R.;
Nuclear Science, IEEE Transactions on
Volume 37, Issue 3, Part 1-2, June 1990 Page(s):1216 - 1221
Digital Object Identifier 10.1109/23.57369
[AbstractPlus](#) | Full Text: [PDF\(576 KB\)](#) IEEE JNL

□ 28. **Simulation and modeling of data acquisition systems for future high energy experiments**
Booth, A.; Black, D.; Walsh, D.; Bowden, M.; Barsotti, E.;
Nuclear Science, IEEE Transactions on
Volume 38, Issue 2, Part 1-2, Apr 1991 Page(s):316 - 321
Digital Object Identifier 10.1109/23.289317
[AbstractPlus](#) | Full Text: [PDF\(536 KB\)](#) IEEE JNL

□ 29. **The synchronous data flow programming language LUSTRE**
Halbwachs, N.; Caspi, P.; Raymond, P.; Pilaud, D.;
Proceedings of the IEEE
Volume 79, Issue 9, Sept. 1991 Page(s):1305 - 1320
Digital Object Identifier 10.1109/5.97300
[AbstractPlus](#) | Full Text: [PDF\(1320 KB\)](#) IEEE JNL

□ 30. **First level calorimeter trigger system for the Large Hadron Collider**
Eisenhandler, E.; Gee, N.; Gillman, A.; Perera, V.; Quinton, S.; Ellis, N.; Fenscon, J.;
Jovanovic, P.; Staley, R.; Watson, A.;
Nuclear Science, IEEE Transactions on
Volume 40, Issue 4, Part 1-2, Aug 1993 Page(s):685 - 687
Digital Object Identifier 10.1109/23.256641
[AbstractPlus](#) | Full Text: [PDF\(272 KB\)](#) IEEE JNL

□ 31. **DAQSIM: a data acquisition system simulation tool**
Booth, A.W.; Botlo, M.; Dorenbosch, J.; Kapoor, V.S.; Milner, E.C.; Wang, C.C.
Nuclear Science, IEEE Transactions on
Volume 40, Issue 4, Part 1-2, Aug 1993 Page(s):788 - 793
Digital Object Identifier 10.1109/23.256662
[AbstractPlus](#) | Full Text: [PDF\(548 KB\)](#) IEEE JNL

□ 32. **A real-time MPEG encoder using a programmable processor**
Kim, D.; Young, J.; Milton, S.; Kim, H.J.; Kim, Y.;
Consumer Electronics, IEEE Transactions on

Volume 40, Issue 2, May 1994 Page(s):161 - 170

Digital Object Identifier 10.1109/30.286411

[AbstractPlus](#) | [Full Text: PDF\(648 KB\)](#) IEEE JNL

- **33. Simulations with SCI as a data carrier in data acquisition systems**
Kristiansen, E.H.; Bothner, J.W.; Hulaas, T.I.; Rongved, E.; Skaali, T.B.; Nuclear Science, IEEE Transactions on
Volume 41, Issue 1, Part 1-2, Feb 1994 Page(s):125 - 130
Digital Object Identifier 10.1109/23.281472
[AbstractPlus](#) | [Full Text: PDF\(532 KB\)](#) IEEE JNL
- **34. Industrial BIST of embedded RAMs**
Camurati, P.; Prinetto, P.; Reorda, M.S.; Barbagallo, S.; Burri, A.; Medina, D.; Design & Test of Computers, IEEE
Volume 12, Issue 3, Autumn/Fall 1995 Page(s):86
Digital Object Identifier 10.1109/MDT.1995.466385
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(800 KB\)](#) IEEE JNL
- **35. Embedded parallel divide-and-conquer video decompression algorithm a for HDTV applications**
Neogi, R.; Saha, A.; Consumer Electronics, IEEE Transactions on
Volume 41, Issue 1, Feb. 1995 Page(s):160 - 171
Digital Object Identifier 10.1109/30.370323
[AbstractPlus](#) | [Full Text: PDF\(820 KB\)](#) IEEE JNL
- **36. High-level modeling and design of asynchronous interface logic**
Yakovlev, A.V.; Koelmans, A.M.; Lavagno, L.; Design & Test of Computers, IEEE
Volume 12, Issue 1, Spring 1995 Page(s):32 - 40
Digital Object Identifier 10.1109/54.350688
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(652 KB\)](#) IEEE JNL
- **37. RPM: a rapid prototyping engine for multiprocessor systems**
Barroso, L.A.; Iman, S.; Dubois, M.; Ramamurthy, K.; Computer
Volume 28, Issue 2, Feb. 1995 Page(s):26 - 34
Digital Object Identifier 10.1109/2.347997
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(888 KB\)](#) IEEE JNL
- **38. Simulating multimedia systems with MVPSIM**
Jihong Kim; Yongmin Kim; Design & Test of Computers, IEEE
Volume 12, Issue 4, Winter 1995 Page(s):18 - 27
Digital Object Identifier 10.1109/54.491234
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(3048 KB\)](#) IEEE JNL
- **39. The design of the microarchitecture of UltraSPARC-I**
Tremblay, M.; Greenley, D.; Normoyle, K.; Proceedings of the IEEE
Volume 83, Issue 12, Dec. 1995 Page(s):1653 - 1663
Digital Object Identifier 10.1109/5.476081
[AbstractPlus](#) | [Full Text: PDF\(1208 KB\)](#) IEEE JNL
- **40. MEC3-a pipelined zero suppression and trigger matching chip**
Mota, M.; Gomes, P.; Christiansen, J.; Nuclear Science, IEEE Transactions on
Volume 42, Issue 4, Part 1-2, Aug 1995 Page(s):808 - 811
Digital Object Identifier 10.1109/23.467884
[AbstractPlus](#) | [Full Text: PDF\(364 KB\)](#) IEEE JNL

- 41. **Fully parallel stochastic computation architecture**
Janer, C.L.; Quero, J.M.; Ortega, J.G.; Franquelo, L.G.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on]
Volume 44, Issue 8, Aug. 1996 Page(s):2110 - 2117
Digital Object Identifier 10.1109/78.533736
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(548 KB) IEEE JNL
- 42. **Developing the AMD-K5 architecture**
Christie, D.;
Micro, IEEE
Volume 16, Issue 2, April 1996 Page(s):16 - 27
Digital Object Identifier 10.1109/40.491459
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1200 KB) IEEE JNL
- 43. **Hardware/software co-design of digital telecommunication systems**
Bolsens, I.; De Man, H.J.; Lin, B.; Van Rompaey, K.; Vercauteren, S.; Verkest, W.
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):391 - 418
Digital Object Identifier 10.1109/5.558713
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(452 KB) IEEE JNL
- 44. **Hardware/software co-design**
De Micheli, G.; Gupta, R.K.;
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):349 - 365
Digital Object Identifier 10.1109/5.558708
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(252 KB) IEEE JNL
- 45. **Circuit techniques in a 266-MHz MMX-enabled processor**
Draper, D.; Crowley, M.; Holst, J.; Favor, G.; Schoy, A.; Trull, J.; Ben-Meir, A.;
Wendell, D.; Krishna, R.; Nolan, J.; Mallick, D.; Partovi, H.; Roberts, M.; Johns, R.
Solid-State Circuits, IEEE Journal of
Volume 32, Issue 11, Nov. 1997 Page(s):1650 - 1664
Digital Object Identifier 10.1109/4.641685
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(328 KB) IEEE JNL
- 46. **A video encoder/decoder architecture for consumer-use HD-DVCRs**
Sang Ju An; Heung Chul Oh; Tae Young Lee; Yong Hwan Lee; Yong Surk Lee
Consumer Electronics, IEEE Transactions on
Volume 43, Issue 3, Aug. 1997 Page(s):352 - 359
Digital Object Identifier 10.1109/30.628624
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(964 KB) IEEE JNL
- 47. **A flexible DSP core for embedded systems**
Kuulusa, M.; Nurmi, J.; Takala, J.; Ojala, P.; Herranen, H.;
Design & Test of Computers, IEEE
Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):60 - 68
Digital Object Identifier 10.1109/54.632882
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(172 KB) IEEE JNL
- 48. **A framework for comparing models of computation**
Lee, E.A.; Sangiovanni-Vincentelli, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 17, Issue 12, Dec. 1998 Page(s):1217 - 1229
Digital Object Identifier 10.1109/43.736561
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(372 KB) IEEE JNL
- 49. **Low-power signal processing system design for wireless applications**
Meng, T.H.; Hung, A.C.; Tsern, E.K.; Gordon, B.M.;
Personal Communications, IEEE [see also IEEE Wireless Communications]
Volume 5, Issue 3, June 1998 Page(s):20 - 31

Digital Object Identifier 10.1109/98.683731

[AbstractPlus](#) | Full Text: [PDF\(2904 KB\)](#) IEEE JNL

50. Testing big chips becomes an internal affair

Runyon, S.;

Spectrum, IEEE

Volume 36, Issue 4, April 1999 Page(s):49 - 55

Digital Object Identifier 10.1109/6.755441

[AbstractPlus](#) | Full Text: [PDF\(1004 KB\)](#) IEEE JNL



[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -

Indexed by




[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Help](#)

Welcome United States Patent and Trademark Office

 [Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE Xplore Guide](#)

Results for "((fifo<and>simulation)<and>vhdl) <and> (pyr >= 1951 <and> pyr <= 2001)"

Your search matched 165 of 1253851 documents.

[e-mail](#)A maximum of 250 results are displayed, 50 to a page, sorted by **Relevance** in **Descending order**.[» Search Options](#)[View Session History](#)[New Search](#)**Modify Search**

[»](#) Check to search only within this results setDisplay Format: Citation Citation & Abstract[» Key](#)[Select](#) Article InformationView: 1-50 | [51-100](#) | [101-165](#)

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

1. **Implementation-independent model of an instruction set architecture in VLSI**
Salinas, M.H.; Johnson, B.W.; Aylor, J.H.;
Design & Test of Computers, IEEE
Volume 10, Issue 3, Sept. 1993 Page(s):42 - 54
Digital Object Identifier 10.1109/54.232471
[AbstractPlus](#) | Full Text: [PDF\(1028 KB\)](#) IEEE JNL

2. **From real-time emulation to ASIC integration for image processing applications**
Kraljic, I.C.; Quenot, G.M.; Zavidovique, B.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 4, Issue 3, Sept. 1996 Page(s):391 - 404
Digital Object Identifier 10.1109/92.532039
[AbstractPlus](#) | References | Full Text: [PDF\(1600 KB\)](#) IEEE JNL

3. **A parallel embedded-processor architecture for ATM reassembly**
Hobson, R.F.; Wong, P.S.;
Networking, IEEE/ACM Transactions on
Volume 7, Issue 1, Feb. 1999 Page(s):23 - 37
Digital Object Identifier 10.1109/90.759314
[AbstractPlus](#) | References | Full Text: [PDF\(328 KB\)](#) IEEE JNL

4. **Top-down design using cycle based simulation: an MPEG A/V decoder example**
Hocevar, D.E.; Ching-Yu Hung; Pickens, D.; Sriram, S.;
VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on
19-21 Feb. 1998 Page(s):400 - 405
Digital Object Identifier 10.1109/GLSV.1998.665333
[AbstractPlus](#) | Full Text: [PDF\(40 KB\)](#) IEEE CNF

5. **Simulation and modeling of a multicast ATM switch**
Siddabathuni, A.C.; Balakrishnan, M.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):242 - 247
Digital Object Identifier 10.1109/ICVD.1999.745155
[AbstractPlus](#) | Full Text: [PDF\(108 KB\)](#) IEEE CNF

6. **Experiences with a versatile prototyping platform for top-down hardware design for communication protocols**
Iselt, A.; Kirstadter, A.;
Performance, Computing, and Communications Conference, 1997. IPCCC 1997
5-7 Feb. 1997 Page(s):385 - 391

Digital Object Identifier 10.1109/PCCC.1997.581542

[AbstractPlus](#) | Full Text: [PDF\(664 KB\)](#) IEEE CNF

- 7. Design of embedded systems: formal models, validation, and synthesis**
Edwards, S.; Lavagno, L.; Lee, E.A.; Sangiovanni-Vincentelli, A.;
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):366 - 390
Digital Object Identifier 10.1109/5.558710
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(252 KB\)](#) IEEE JNL

- 8. A distributed access generic optical network interface for SMDS network**
Shahrier, S.M.; Jenevein, R.M.;
Performance, Computing, and Communications Conference, 1997. IPCCC 1997
International
5-7 Feb. 1997 Page(s):493 - 501
Digital Object Identifier 10.1109/PCCC.1997.581555
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(716 KB\)](#) IEEE CNF

- 9. Profile-driven behavioral synthesis for low-power VLSI systems**
Kumar, N.; Katkoori, S.; Rader, L.; Vemuri, R.;
Design & Test of Computers, IEEE
Volume 12, Issue 3, Autumn/Fall 1995 Page(s):70
Digital Object Identifier 10.1109/MDT.1995.466383
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1044 KB\)](#) IEEE JNL

- 10. SIERA: a unified framework for rapid-prototyping of system-level hardware**
Srivastava, M.; Brodersen, R.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 14, Issue 6, June 1995 Page(s):676 - 693
Digital Object Identifier 10.1109/43.387729
[AbstractPlus](#) | Full Text: [PDF\(1876 KB\)](#) IEEE JNL

- 11. Core design and system-on-a-chip integration**
Rincon, A.M.; Cherichetti, G.; Monzel, J.A.; Stauffer, D.R.; Trick, M.T.;
Design & Test of Computers, IEEE
Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):26 - 35
Digital Object Identifier 10.1109/54.632878
[AbstractPlus](#) | Full Text: [PDF\(228 KB\)](#) IEEE JNL

- 12. Continuously live image processor for drift chamber track segment trigger**
Berenyi, A.; Chen, H.K.; Dao, K.; Dow, S.F.; Gehrig, S.K.; Gill, M.S.; Grace, C.;
Johnson, J.K.; Karcher, A.; Kasen, D.; Kirsten, F.A.; Kral, J.F.; LeClerc, C.M.; Leder Lippe, H.; Liu, T.H.; Marks, K.M.; Meyer, A.B.; Minor, R.; Montgomery, A.H.;
Nuclear Science, IEEE Transactions on
Volume 46, Issue 3, Part 1, June 1999 Page(s):348 - 353
Digital Object Identifier 10.1109/23.775542
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(604 KB\)](#) IEEE JNL

- 13. RPM: a rapid prototyping engine for multiprocessor systems**
Barroso, L.A.; Iman, S.; Dubois, M.; Ramamurthy, K.;
Computer
Volume 28, Issue 2, Feb. 1995 Page(s):26 - 34
Digital Object Identifier 10.1109/2.347997
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(888 KB\)](#) IEEE JNL

- 14. Hardware/software co-design of digital telecommunication systems**
Bolsens, I.; De Man, H.J.; Lin, B.; Van Rompaey, K.; Vercauteren, S.; Verkest, A.;
Proceedings of the IEEE
Volume 85, Issue 3, March 1997 Page(s):391 - 418
Digital Object Identifier 10.1109/5.558713
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(452 KB\)](#) IEEE JNL

15. **Micropipelined asynchronous discrete cosine transform (DCT/IDCT) processor**
Johnson, D.; Akella, V.; Stott, B.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 6, Issue 4, Dec. 1998 Page(s):731 - 740
Digital Object Identifier 10.1109/92.736146
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(192 KB\)](#) IEEE JNL

16. **Hierarchical finite state machines with multiple concurrency models**
Girault, A.; Bilung Lee; Lee, E.A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 18, Issue 6, June 1999 Page(s):742 - 760
Digital Object Identifier 10.1109/43.766725
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(312 KB\)](#) IEEE JNL

17. **A case study in design space exploration: the Tosca environment applied to a telecommunication link controller**
Allara, A.; Bombana, M.; Fornaciari, W.; Salice, F.;
Design & Test of Computers, IEEE
Volume 17, Issue 2, April-June 2000 Page(s):60 - 72
Digital Object Identifier 10.1109/54.844335
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(120 KB\)](#) IEEE JNL

18. **Design space exploration techniques for the codesign of embedded data systems**
Deegener, M.; Huss, S.A.;
Computers and Digital Techniques, IEE Proceedings-Digital Techniques
Volume 145, Issue 3, May 1998 Page(s):161 - 170
[AbstractPlus](#) | Full Text: [PDF\(1592 KB\)](#) IEE JNL

19. **Continuously live image processor for drift chamber track segment trigger**
Berenyi, A.; Chen, H.K.; Dao, K.; Dow, S.F.; Gehrig, S.K.; Gill, M.S.; Grace, C.;
Johnson, J.K.; Karcher, A.; Kasen, D.; Kirsten, F.A.; Kral, J.E.; LeClerc, C.M.;
Der Lippe, H.; Liu, T.H.; Marks, K.M.; Meyer, A.B.; Minor, R.; Montgomery, A.;
Nuclear Science Symposium, 1998. Conference Record. 1998 IEEE
Volume 2, 8-14 Nov. 1998 Page(s):977 - 982 vol.2
Digital Object Identifier 10.1109/NSSMIC.1998.774330
[AbstractPlus](#) | Full Text: [PDF\(528 KB\)](#) IEEE CNF

20. **Using VHDL for high-level, mixed-mode system simulation**
Srivastava, M.B.; Brodersen, R.W.;
Design & Test of Computers, IEEE
Volume 9, Issue 3, Sept. 1992 Page(s):31 - 40
Digital Object Identifier 10.1109/54.156156
[AbstractPlus](#) | Full Text: [PDF\(960 KB\)](#) IEEE JNL

21. **A CMOS IC for Gb/s Viterbi decoding: system design and VLSI implementation**
Dawid, H.; Fettweis, G.; Meyr, H.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 4, Issue 1, March 1996 Page(s):17 - 31
Digital Object Identifier 10.1109/92.486078
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(2028 KB\)](#) IEEE JNL

22. **A cost-effective architecture for HDTV video decoder in ATSC receivers**
Jeong-Min Kim; Soo-Ik Chae;
Consumer Electronics, IEEE Transactions on
Volume 44, Issue 4, Nov. 1998 Page(s):1353 - 1359
Digital Object Identifier 10.1109/30.735837
[AbstractPlus](#) | Full Text: [PDF\(908 KB\)](#) IEEE JNL

23. **Verification of asynchronous circuits with bounded inertial gate delays**
Gong, J.; Wong, E.M.C.;

Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian
2-4 Dec. 1998 Page(s):399 - 401
Digital Object Identifier 10.1109/ATS.1998.741646
[AbstractPlus](#) | Full Text: [PDF](#)(140 KB) IEEE CNF

- **24. OMI-compliant model for virtual emulation**
Dozza, D.; Rambaldi, R.; Borgatti, M.; Guerrieri, R.;
Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Works
3-5 June 1998 Page(s):64 - 69
Digital Object Identifier 10.1109/IWRSP.1998.676670
[AbstractPlus](#) | Full Text: [PDF](#)(148 KB) IEEE CNF
- **25. The STAR cluster-finder ASIC**
Botto, M.; LeVine, M.J.; Scheetz, R.A.; Schulz, M.W.; Short, P.; Woods, J.; CRC
Nuclear Science, IEEE Transactions on
Volume 45, Issue 4, Part 1, Aug. 1998 Page(s):1809 - 1813
Digital Object Identifier 10.1109/23.710941
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(440 KB) IEEE JNL
- **26. Semicustom design of an IEEE 1394-compliant reusable IC core**
Bertacchi, M.; Grossi, D.; De Gloria, A.; Olivieri, M.;
Design & Test of Computers, IEEE
Volume 17, Issue 3, July-Sept. 2000 Page(s):95 - 105
Digital Object Identifier 10.1109/54.867900
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(116 KB) IEEE JNL
- **27. The architecture of a processor array for video decompression**
Mayer, A.C.;
Consumer Electronics, IEEE Transactions on
Volume 39, Issue 3, Aug. 1993 Page(s):565 - 569
Digital Object Identifier 10.1109/30.234636
[AbstractPlus](#) | Full Text: [PDF](#)(328 KB) IEEE JNL
- **28. The digital ASIC for the Digital Front End Electronics of the SPI astrophysics experiment**
Lafond, E.; Mur, M.; Schanne, S.;
Nuclear Science, IEEE Transactions on
Volume 45, Issue 4, Part 1, Aug. 1998 Page(s):1836 - 1839
Digital Object Identifier 10.1109/23.710946
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(344 KB) IEEE JNL
- **29. A hardware-oriented gold-washing adaptive vector quantizer and its VLSI for image data compression**
Shaou-Gang Miaou; Wen-Song Chung;
Circuits and Systems for Video Technology, IEEE Transactions on
Volume 10, Issue 8, Dec. 2000 Page(s):1502 - 1513
Digital Object Identifier 10.1109/76.889060
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(280 KB) IEEE JNL
- **30. Using general-purpose programming languages for FPGA design**
Hutchings, B.L.; Nelson, B.E.;
Design Automation Conference, 2000. Proceedings 2000. 37th
June 5-9, 2000 Page(s):561 - 566
[AbstractPlus](#) | Full Text: [PDF](#)(648 KB) IEEE CNF
- **31. Hardware architecture for optical flow estimation in real time**
Zuloaga, A.; Martin, J.L.; Ezquerro, J.;
Image Processing, 1998. ICIP 98. Proceedings. 1998 International Conference
4-7 Oct. 1998 Page(s):972 - 976 vol.3
Digital Object Identifier 10.1109/ICIP.1998.727412
[AbstractPlus](#) | Full Text: [PDF](#)(483 KB) IEEE CNF

- 32. An asynchronous implementation of the maxlist algorithm
Myers, C.J.; Hao Zheng;
Acoustics, Speech, and Signal Processing, 1997. ICASSP-97., 1997 IEEE Inte Conference on
Volume 1, 21-24 April 1997 Page(s):647 - 650 vol.1
Digital Object Identifier 10.1109/ICASSP.1997.599851
[AbstractPlus](#) | Full Text: [PDF\(320 KB\)](#) IEEE CNF
- 33. A multithreaded processor designed for distributed shared memory syst
Grunewald, W.; Ungerer, T.;
Advances in Parallel and Distributed Computing, 1997. Proceedings 19-21 March 1997 Page(s):206 - 213
Digital Object Identifier 10.1109/APDC.1997.574034
[AbstractPlus](#) | Full Text: [PDF\(864 KB\)](#) IEEE CNF
- 34. Architectural considerations for a self-timed decoupled processor
Richardson, W.F.; Brunvand, E.;
Computers and Digital Techniques, IEE Proceedings- Volume 143, Issue 5, Sept. 1996 Page(s):251 - 258
[AbstractPlus](#) | Full Text: [PDF\(652 KB\)](#) IEE JNL
- 35. Embedded parallel divide-and-conquer video decompression algorithm a for HDTV applications
Neogi, R.; Saha, A.;
Consumer Electronics, IEEE Transactions on Volume 41, Issue 1, Feb. 1995 Page(s):160 - 171
Digital Object Identifier 10.1109/30.370323
[AbstractPlus](#) | Full Text: [PDF\(820 KB\)](#) IEEE JNL
- 36. Design of a static MIMD data flow processor using micropipelines
Chih-Ming Chang; Shih-Lien Lu;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 3, Issue 3, Sept. 1995 Page(s):370 - 378
Digital Object Identifier 10.1109/92.406995
[AbstractPlus](#) | Full Text: [PDF\(756 KB\)](#) IEEE JNL
- 37. Conceptual prototyping of scalable embedded DSP systems
Dung, L.-R.; Madisetti, V.K.;
Design & Test of Computers, IEEE Volume 13, Issue 3, Fall 1996 Page(s):54 - 65
Digital Object Identifier 10.1109/54.536096
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(2464 KB\)](#) IEEE JNL
- 38. Analysis and synthesis of concurrent digital circuits using control-flow e Coelho, C.N., Jr.; De Micheli, G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 15, Issue 8, Aug. 1996 Page(s):854 - 876
Digital Object Identifier 10.1109/43.511567
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(2248 KB\)](#) IEEE JNL
- 39. Computer-aided verification
Clarke, E.M.; Kurshan, R.P.;
Spectrum, IEEE Volume 33, Issue 6, June 1996 Page(s):61 - 67
Digital Object Identifier 10.1109/6.499951
[AbstractPlus](#) | Full Text: [PDF\(2316 KB\)](#) IEEE JNL
- 40. Programmable active memories: reconfigurable systems come of age Vuillemin, J.E.; Bertin, P.; Roncin, D.; Shand, M.; Touati, H.H.; Boucard, P.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 4, Issue 1, March 1996 Page(s):56 - 69

Digital Object Identifier 10.1109/92.486081

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1588 KB\)](#) IEEE JNL

- 41. **Design of an ASIP architecture for low-level visual elaborations**
Raffo, L.; Sabatini, S.P.; Mantelli, M.; De Gloria, A.; Bisio, G.M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 5, Issue 1, March 1997 Page(s):145 - 153
Digital Object Identifier 10.1109/92.555994
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(192 KB\)](#) IEEE JNL
- 42. **A framework for comparing models of computation**
Lee, E.A.; Sangiovanni-Vincentelli, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 17, Issue 12, Dec. 1998 Page(s):1217 - 1229
Digital Object Identifier 10.1109/43.736561
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(372 KB\)](#) IEEE JNL
- 43. **Design of a scan format converter using the bisigmoidal interpolation**
Jaejun Lee; Yunmo Chung; Chae-Gon Oh; Jin-Goo Kim; Chang-Wan Hong;
Consumer Electronics, IEEE Transactions on
Volume 44, Issue 3, Aug. 1998 Page(s):1115 - 1121
Digital Object Identifier 10.1109/30.713243
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(448 KB\)](#) IEEE JNL
- 44. **Translucent smart pixel array (TRANSPAR) chips for high throughput net
signal processing**
Chen, C.-H.; Hoanca, B.; Kuznia, C.B.; Sawchuk, A.A.; Wu, J.-M.;
Selected Topics in Quantum Electronics, IEEE Journal of
Volume 5, Issue 2, March-April 1999 Page(s):316 - 329
Digital Object Identifier 10.1109/2944.778315
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(776 KB\)](#) IEEE JNL
- 45. **A video segmentation algorithm for hierarchical object representations a
implementation**
Herrmann, S.; Mooshofer, H.; Dietrich, H.; Stechele, W.;
Circuits and Systems for Video Technology, IEEE Transactions on
Volume 9, Issue 8, Dec. 1999 Page(s):1204 - 1215
Digital Object Identifier 10.1109/76.809156
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(644 KB\)](#) IEEE JNL
- 46. **Accelerating Markovian analysis of asynchronous systems using state c
Aiguo Xie; Beerel, P.A.;**
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 18, Issue 7, July 1999 Page(s):869 - 888
Digital Object Identifier 10.1109/43.771173
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(372 KB\)](#) IEEE JNL
- 47. **Modeling and simulation of a readout architecture for pixel detectors**
Cancelo, G.I.E.; Zimmermann, S.;
Nuclear Science, IEEE Transactions on
Volume 47, Issue 6, Part 2, Dec. 2000 Page(s):2007 - 2013
Digital Object Identifier 10.1109/23.903837
[AbstractPlus](#) | Full Text: [PDF\(484 KB\)](#) IEEE JNL
- 48. **An efficient cell-scheduling algorithm for multicast ATM switching system**
Wen-Tsuen Chen; Chun-Fu Huang; Yi-Luang Chang; Wu-Yuin Hwang;
Networking, IEEE/ACM Transactions on
Volume 8, Issue 4, Aug. 2000 Page(s):517 - 525
Digital Object Identifier 10.1109/90.865079
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(256 KB\)](#) IEEE JNL

49. **Design methodology for a large communication chip**
Clauberg, R.; Buchmann, P.; Herkersdorf, A.; Webb, D.J.;
Design & Test of Computers, IEEE
Volume 17, Issue 3, July-Sept. 2000 Page(s):86 - 94
Digital Object Identifier 10.1109/54.867899
[Abstract](#)[Plus](#) | [References](#) | [Full Text: PDF\(104 KB\)](#) | [IEEE JNL](#)

50. **Designing electronic engines with electronic engines: 40 years of bootstrap technology upon itself**
Jess, J.A.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1404 - 1427
Digital Object Identifier 10.1109/43.898824
[Abstract](#)[Plus](#) | [References](#) | [Full Text: PDF\(280 KB\)](#) | [IEEE JNL](#)

[View: 1-50](#) | [51-100](#) | [...](#)

Indexed by
 Inspec®

[Help](#) | [Contact Us](#) | [Privacy & Terms](#)
© Copyright 2005 IEEE -


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

□ Search Results

[BROWSE](#)[SEARCH](#)[IEEE Xplore Guide](#)

Results for "((tri-state<and>simulation)<and>vhdl) <and> (pyr >= 1951 <and> pyr <= ..."

[e-mail](#)

Your search matched 37 of 1253851 documents.

A maximum of 250 results are displayed, 50 to a page, sorted by **Relevance** in **Descending** order.» [Search Options](#)[View Session History](#)[New Search](#)

Modify Search

»
 Check to search only within this results set
Display Format: Citation Citation & Abstract» [Key](#)

IEEE JNL IEEE Journal or Magazine

[Select](#)[Article Information](#)

IEE JNL IEE Journal or Magazine

 1. **IEEE standard for VITAL ASIC (application specific integrated circuit) m**
specification

IEEE Std 1076.4-2000

2001 Page(s):0_1 - 420

[AbstractPlus](#) | [Full Text: PDF\(1376 KB\)](#) IEEE STD

IEEE CNF IEE Conference Proceeding

 2. **VHDL and top-down methods prove successful in automotive electronic**
Halwood, M.A.;
Computer Aided Engineering of Automotive Electronics, IEE Colloquium on
27 Apr 1994 Page(s):8/1 - 810
[AbstractPlus](#) | [Full Text: PDF\(404 KB\)](#) IEE CNF

IEEE STD IEEE Standard

 3. **High-performance energy-efficient D-flip-flop circuits**
Uming Ko; Balsara, P.T.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 8, Issue 1, Feb. 2000 Page(s):94 - 98
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(148 KB\)](#) IEEE JNL
 4. **Multi-signal flow graphs: a novel approach for system testability analysis**
diagnosis
Deb, S.; Pattipati, K.R.; Raghavan, V.; Shakeri, M.; Shrestha, R.;

Aerospace and Electronic Systems Magazine, IEEE

Volume 10, Issue 5, May 1995 Page(s):14 - 25

Digital Object Identifier 10.1109/92.820765

[AbstractPlus](#) | [Full Text: PDF\(1064 KB\)](#) IEEE JNL
 5. **Methods of exploiting simulation technology for simulating the timing of**
reconfigurable logic
Robinson, D.; Lysaght, P.;

Computers and Digital Techniques, IEE Proceedings-

Volume 147, Issue 3, May 2000 Page(s):175 - 180

Digital Object Identifier 10.1049/ip-cdt:20000498

[AbstractPlus](#) | [Full Text: PDF\(532 KB\)](#) IEE JNL
 6. **Assertion checking by combined word-level ATPG and modular arithmetic**
solving techniques
Chung-Yang Huang; Kwang-Ting Cheng;

Design Automation Conference, 2000. Proceedings 2000. 37th

June 5-9, 2000 Page(s):118 - 123

[AbstractPlus](#) | [Full Text: PDF\(612 KB\)](#) IEEE CNF

- 7. **Modeling and analysis of the difference-bit cache**
Kulkarni, A.; Chander, N.; Pillai, S.; John, L.;
VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on
19-21 Feb. 1998 Page(s):140 - 145
Digital Object Identifier 10.1109/GLSV.1998.665215
[AbstractPlus](#) | Full Text: [PDF\(44 KB\)](#) IEEE JNL
- 8. **Design and application of an optimizing XROM silicon compiler**
Linderman, R.W.; Rossbach, P.C.; Gallagher, D.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 8, Issue 12, Dec. 1989 Page(s):1267 - 1275
Digital Object Identifier 10.1109/43.44507
[AbstractPlus](#) | Full Text: [PDF\(1104 KB\)](#) IEEE JNL
- 9. **The Test Engineer's Assistant: a design environment for testable and dia systems**
Hallenbeck, J.J.; Kanopoulos, N.; Cybrynski, J.R.;
Industrial Electronics, IEEE Transactions on
Volume 36, Issue 2, May 1989 Page(s):278 - 285
Digital Object Identifier 10.1109/41.19079
[AbstractPlus](#) | Full Text: [PDF\(704 KB\)](#) IEEE JNL
- 10. **START: System Testability Analysis and Research Tool**
Pattipati, K.R.; Deb, S.; Dontamsetty, M.; Maitra, A.;
Aerospace and Electronic Systems Magazine, IEEE
Volume 6, Issue 1, Jan. 1991 Page(s):13 - 20
Digital Object Identifier 10.1109/62.64988
[AbstractPlus](#) | Full Text: [PDF\(756 KB\)](#) IEEE JNL
- 11. **Codesign of communication protocols**
Wenban, A.S.; O'Leary, J.W.; Brown, G.M.;
Computer
Volume 26, Issue 12, Dec. 1993 Page(s):46 - 52
Digital Object Identifier 10.1109/2.247651
[AbstractPlus](#) | Full Text: [PDF\(696 KB\)](#) IEEE JNL
- 12. **Microprocessors and digital ICs for motion control**
Hoang Le-Huy;
Proceedings of the IEEE
Volume 82, Issue 8, Aug. 1994 Page(s):1140 - 1163
Digital Object Identifier 10.1109/5.301682
[AbstractPlus](#) | Full Text: [PDF\(2132 KB\)](#) IEEE JNL
- 13. **Seventh IEEE International Conference on Wafer Scale Integration**
Components, Packaging, and Manufacturing Technology, Part B: Advanced P. Transactions on [see also Components, Hybrids, and Manufacturing Technolo Transactions on]
Volume 18, Issue 3, Aug 1995
Digital Object Identifier 10.1109/96.407073
[AbstractPlus](#) | Full Text: [PDF\(4516 KB\)](#) IEEE JNL
- 14. **SIERA: a unified framework for rapid-prototyping of system-level hardwa**
Srivastava, M.; Brodersen, R.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 14, Issue 6, June 1995 Page(s):676 - 693
Digital Object Identifier 10.1109/43.387729
[AbstractPlus](#) | Full Text: [PDF\(1876 KB\)](#) IEEE JNL
- 15. **A hybrid-SEED smart pixel array for a four-stage intelligent optical backp demonstrator**
Rolston, D.R.; Plant, D.V.; Szymanski, T.H.; Hinton, H.S.; Hsiao, W.S.; Ayliffe,

Venditti, M.B.; Desai, P.; Krishnamoorthy, A.V.; Goossen, K.W.; Walker, J.A.; S.P.; Cunningham, J.E.; Jan, W.Y.; Selected Topics in Quantum Electronics, IEEE Journal of Volume 2, Issue 1, April 1996 Page(s):97 - 105 Digital Object Identifier 10.1109/2944.541878
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1064 KB\)](#) | [IEEE JNL](#)

- 16. Rule checking at the register level**
Caporossi, D.; Marschner, F.E.; Read, S.; Spectrum, IEEE Volume 33, Issue 6, June 1996 Page(s):72 - 73 Digital Object Identifier 10.1109/6.499957
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(536 KB\)](#) | [IEEE JNL](#)
- 17. Ravel-XL: a hardware accelerator for assigned-delay compiled-code logic**
Riepe, M.A.; Silva, J.P.M.; Sakallah, K.A.; Brown, R.B.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 4, Issue 1, March 1996 Page(s):113 - 129 Digital Object Identifier 10.1109/92.486085
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1884 KB\)](#) | [IEEE JNL](#)
- 18. An evaluation of parallel simulated annealing strategies with application placement**
Chandy, J.A.; Sungho Kim; Ramkumar, B.; Parkes, S.; Banerjee, P.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 16, Issue 4, April 1997 Page(s):398 - 410 Digital Object Identifier 10.1109/43.602476
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(308 KB\)](#) | [IEEE JNL](#)
- 19. On-line fault detection for bus-based field programmable gate arrays**
Shnidman, N.R.; Mangione-Smith, W.H.; Potkonjak, M.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 6, Issue 4, Dec. 1998 Page(s):656 - 666 Digital Object Identifier 10.1109/92.736139
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(332 KB\)](#) | [IEEE JNL](#)
- 20. Efficient algorithm and architecture for post-processor in HDTV**
Jae-Wook Lee; Jeong-Woo Park; Myung-Hoon Yang; Sungho Kang; Yoonsik Kim; Consumer Electronics, IEEE Transactions on Volume 44, Issue 1, Feb. 1998 Page(s):16 - 26 Digital Object Identifier 10.1109/30.663726
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1164 KB\)](#) | [IEEE JNL](#)
- 21. A scan-based configurable, programmable, and scalable architecture for scan-based operations**
Thibeault, C.; Begin, G.; Computers, IEEE Transactions on Volume 48, Issue 6, June 1999 Page(s):615 - 627 Digital Object Identifier 10.1109/12.773798
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(748 KB\)](#) | [IEEE JNL](#)
- 22. C-based SoC design flow and EDA tools: an ASIC and system vendor perspective**
Wakabayashi, K.; Okamoto, T.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522 Digital Object Identifier 10.1109/43.898829
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(388 KB\)](#) | [IEEE JNL](#)
- 23. FPGA prototyping of a RISC processor core for embedded applications**
Gschwind, M.; Salapura, V.; Maurer, D.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 9, Issue 2, April 2001 Page(s):241 - 250

Digital Object Identifier 10.1109/92.924027

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(436 KB\)](#) IEEE JNL

- **24. System-on-chip testability using LSSD scan structures**
Zarrineh, K.; Upadhyaya, S.J.; Chickermane, V.;
Design & Test of Computers, IEEE
Volume 18, Issue 3, May-June 2001 Page(s):83 - 97
Digital Object Identifier 10.1109/54.922805
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(156 KB\)](#) IEEE JNL
- **25. Fully integrated standard cell digital PLL**
Olsson, T.; Nilsson, P.;
Electronics Letters
Volume 37, Issue 4, 15 Feb 2001 Page(s):211 - 212
Digital Object Identifier 10.1049/el:20010160
[AbstractPlus](#) | Full Text: [PDF\(200 KB\)](#) IEE JNL
- **26. RC op-amp implementation of hysteresis chaotic oscillator**
Bizzarri, F.; Storace, M.;
Electronics Letters
Volume 37, Issue 4, 15 Feb 2001 Page(s):209 - 211
Digital Object Identifier 10.1049/el:20010148
[AbstractPlus](#) | Full Text: [PDF\(304 KB\)](#) IEE JNL
- **27. Embedded hardware and software self-testing methodologies for processes**
Li Chen; Dey, S.; Sanchez, P.; Sekar, K.; Ying Chen;
Design Automation Conference, 2000. Proceedings 2000. 37th
June 5-9, 2000 Page(s):625 - 630
[AbstractPlus](#) | Full Text: [PDF\(668 KB\)](#) IEEE CNF
- **28. A low-voltage low-power high performance fully integrated DTMF receiver**
Vazquez, D.; Avedillo, M.J.; Huertas, G.; Quintana, J.M.; Pauritsch, M.; Rueda
J.L.;
Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27
18-20 Sept. 2001 Page(s):353 - 356
[AbstractPlus](#) | Full Text: [PDF\(112 KB\)](#) IEEE CNF
- **29. SOM hardware with acceleration module for graphical representation of 1D and 2D processes**
Porrmann, M.; Ruping, S.; Ruckert, U.;
Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999. MicroNeu
Proceedings of the Seventh International Conference on
7-9 April 1999 Page(s):380 - 386
Digital Object Identifier 10.1109/MN.1999.758890
[AbstractPlus](#) | Full Text: [PDF\(124 KB\)](#) IEEE CNF
- **30. Architecture and design of GE1, an FCCM for Golomb ruler derivation**
Dellas, A.; Sotiriades, E.; Emmanouelides, A.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium
15-17 April 1998 Page(s):48 - 56
Digital Object Identifier 10.1109/FPGA.1998.707880
[AbstractPlus](#) | Full Text: [PDF\(64 KB\)](#) IEEE CNF
- **31. A flexible pipelined image processor**
Kelly, M.; Hsu, K.W.;
ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International
13-16 Sept. 1998 Page(s):325 - 332
Digital Object Identifier 10.1109/ASIC.1998.723026
[AbstractPlus](#) | Full Text: [PDF\(844 KB\)](#) IEEE CNF
- **32. Test methodology for a microprocessor with partial scan**

Day, L.L.; Ganfield, P.A.; Rickert, D.M.; Ziegler, F.J.;
Test Conference, 1998. Proceedings. International
18-23 Oct. 1998 Page(s):708 - 716
Digital Object Identifier 10.1109/TEST.1998.743215
[AbstractPlus](#) | Full Text: [PDF\(788 KB\)](#) IEEE CNF

□ 33. An extensible, low cost rapid prototyping environment based on a recon^{fgurable} FPGAs
Adaos, K.; Alexiou, G.P.; Kanopoulos, N.;
Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Works
3-5 June 1998 Page(s):78 - 83
Digital Object Identifier 10.1109/IWRSP.1998.676672
[AbstractPlus](#) | Full Text: [PDF\(104 KB\)](#) IEEE CNF

□ 34. A reconfigurable logic machine for fast event-driven simulation
Bauer, J.; Bershteyn, M.; Kaplan, I.; Vyedin, P.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):668 - 671
[AbstractPlus](#) | Full Text: [PDF\(372 KB\)](#) IEEE CNF

□ 35. The requirements for a VHDL based custom IC, ASIC or FPGA design prc
Collis, S.D.;
VHDL (Very High Speed Integrated Circuits Hardware Description Language).
CAE Advances, IEE Colloquium on (Digest No.1993/076)
6 Apr 1993 Page(s):7/1 - 7/7
[AbstractPlus](#) | Full Text: [PDF\(388 KB\)](#) IEE CNF

□ 36. IEEE standard for VITAL Application-Specific Integrated Circuit (ASIC) m
specification
IEEE Std 1076.4-1995
17 May 1996
[AbstractPlus](#) | Full Text: [PDF\(3828 KB\)](#) IEEE STD

□ 37. IEEE standard multivalue logic system for VHDL model interoperability
(Std_logic_1164)
IEEE Std 1164-1993
26 May 1993
[AbstractPlus](#) | Full Text: [PDF\(312 KB\)](#) IEEE STD


 [Search Results](#)
[BROWSE](#)
[SEARCH](#)
[IEEE Xplore Guide](#)

Results for "((tri-state<and>simulation)<and>verilog) <and> (pyr >= 1951 <and> pyr <...)"

[e-mail](#)

Your search matched 25 of 1253851 documents.

 A maximum of 250 results are displayed, 50 to a page, sorted by **Relevance** in **Descending** order.

 » [Search Options](#)
[View Session History](#)
[New Search](#)

Modify Search

 (((tri-state<and>simulation)<and>verilog) <and> (pyr >= 1951 <and> pyr <= 2001)) [»](#)
 Check to search only within this results set

 Display Format: Citation Citation & Abstract

 » [Key](#)
IEEE JNL IEEE Journal or Magazine

Select Article Information

IEE JNL IEE Journal or Magazine

1. **IEEE standard hardware description language based on the Verilog(R) ha**
description language

IEEE Std 1364-1995

14 Oct. 1996

[AbstractPlus](#) | [Full Text: PDF\(6360 KB\)](#) IEEE STD

IEEE STD IEEE Standard

2. **Ravel-XL: a hardware accelerator for assigned-delay compiled-code logic**
 Riepe, M.A.; Silva, J.P.M.; Sakallah, K.A.; Brown, R.B.;

 Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
 Volume 4, Issue 1, March 1996 Page(s):113 - 129
 Digital Object Identifier 10.1109/92.486085

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1884 KB\)](#) IEEE JNL

3. **An approach to verify a large scale system-on-a-chip using symbolic mo**
 Takayama, K.; Satoh, T.; Nakata, T.; Hirose, F.;

 Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proce
 International Conference on
 5-7 Oct. 1998 Page(s):308 - 313
 Digital Object Identifier 10.1109/ICCD.1998.727066

[AbstractPlus](#) | [Full Text: PDF\(96 KB\)](#) IEEE CNF

4. **Mixed 2-4 state simulation with VCS**

 Chaudhry, H.K.; Eichenberger, P.; Chowdhury, D.R.;
 Verilog HDL Conference, 1997., IEEE International
 31 March-2 April 1997 Page(s):77 - 82
 Digital Object Identifier 10.1109/IVC.1997.588537

[AbstractPlus](#) | [Full Text: PDF\(392 KB\)](#) IEEE CNF

5. **A multiple-strength multiple-delay compiled-code logic simulator**

 Parlakbilek, A.N.; Lewis, D.M.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
 Volume 12, Issue 12, Dec. 1993 Page(s):1937 - 1946
 Digital Object Identifier 10.1109/43.251157

[AbstractPlus](#) | [Full Text: PDF\(996 KB\)](#) IEEE JNL

6. **Benchmark circuits improve the quality of a standard cell library**

 Rung-Bin Lin; Isaac Shuo-Hsiu Chou; Chi-Ming Tsai;
 Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia
 18-21 Jan. 1999 Page(s):173 - 176 vol.1
 Digital Object Identifier 10.1109/ASPDAC.1999.759988

[AbstractPlus](#) | [Full Text: PDF\(360 KB\)](#) IEEE CNF

- 7. Enhanced visibility and performance in functional verification by reconst
Marantz, J.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):164 - 169
[AbstractPlus](#) | [Full Text: PDF\(512 KB\)](#) | [IEEE CNF](#)

- 8. Dynamic power management for microprocessors: a case study
Tiwari, V.; Donnelly, R.; Malik, S.; Gonzalez, R.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):185 - 192
Digital Object Identifier 10.1109/ICVD.1997.568074
[AbstractPlus](#) | [Full Text: PDF\(924 KB\)](#) | [IEEE CNF](#)

- 9. IEEE standard Verilog hardware description language
IEEE Std 1364-2001
2001 Page(s):0_1 - 856
[AbstractPlus](#) | [Full Text: PDF\(3773 KB\)](#) | [IEEE STD](#)

- 10. Microprocessors and digital ICs for motion control
Hoang Le-Huy;
Proceedings of the IEEE
Volume 82, Issue 8, Aug. 1994 Page(s):1140 - 1163
Digital Object Identifier 10.1109/5.301682
[AbstractPlus](#) | [Full Text: PDF\(2132 KB\)](#) | [IEEE JNL](#)

- 11. A new self-routing permutation network
Wang-Jiunn Cheng; Wen-Tsuen Chen;
Computers, IEEE Transactions on
Volume 45, Issue 5, May 1996 Page(s):630 - 636
Digital Object Identifier 10.1109/12.509917
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(676 KB\)](#) | [IEEE JNL](#)

- 12. Rule checking at the register level
Caporossi, D.; Marschner, F.E.; Read, S.;
Spectrum, IEEE
Volume 33, Issue 6, June 1996 Page(s):72 - 73
Digital Object Identifier 10.1109/6.499957
[AbstractPlus](#) | [Full Text: PDF\(536 KB\)](#) | [IEEE JNL](#)

- 13. Partitioning and analysis of static digital CMOS circuits
Hubner, U.; Vierhaus, H.T.; Camposano, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 16, Issue 11, Nov. 1997 Page(s):1292 - 1310
Digital Object Identifier 10.1109/43.663819
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(548 KB\)](#) | [IEEE JNL](#)

- 14. C-based SoC design flow and EDA tools: an ASIC and system vendor perspective
Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522
Digital Object Identifier 10.1109/43.898829
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(388 KB\)](#) | [IEEE JNL](#)

- 15. A low latency architecture for computing multiplicative inverses and divisions
Dinh, A.V.; Bolton, R.J.; Mason, R.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transaction
Circuits and Systems II: Express Briefs, IEEE Transactions on
Volume 48, Issue 8, Aug. 2001 Page(s):789 - 793
Digital Object Identifier 10.1109/82.959871
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(160 KB\)](#) | [IEEE JNL](#)

- 16. **Architecture and design of NX-2700: a programmable single-chip HDTV a decode-and-display processor**
Dutta, S.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 9, Issue 2, April 2001 Page(s):313 - 328
Digital Object Identifier 10.1109/92.924054
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(232 KB\)](#) | [IEEE JNL](#)
- 17. **Methods of exploiting simulation technology for simulating the timing of reconfigurable logic**
Robinson, D.; Lysaght, P.;
Computers and Digital Techniques, IEE Proceedings- Volume 147, Issue 3, May 2000 Page(s):175 - 180
Digital Object Identifier 10.1049/ip-cdt:20000498
[AbstractPlus](#) | [Full Text: PDF\(532 KB\)](#) | [IEE JNL](#)
- 18. **In-sawing-lane multi-level BIST for known good dies of LCD drivers**
Chua-Chin Wang; Chi-Feng Wu; Sheng-Hua Chen; Chia-Hsiung Kao; Electronics Letters Volume 35, Issue 18, 2 Sept. 1999 Page(s):1543 - 1544
Digital Object Identifier 10.1049/el:19991057
[AbstractPlus](#) | [Full Text: PDF\(292 KB\)](#) | [IEE JNL](#)
- 19. **Assertion checking by combined word-level ATPG and modular arithmetic solving techniques**
Chung-Yang Huang; Kwang-Ting Cheng;
Design Automation Conference, 2000. Proceedings 2000. 37th June 5-9, 2000 Page(s):118 - 123
[AbstractPlus](#) | [Full Text: PDF\(612 KB\)](#) | [IEEE CNF](#)
- 20. **CGaAs PowerPC FXU**
Drake, A.J.; Basso, T.D.; Gold, S.M.; Kraver, K.L.; Parakh, P.N.; Gauthier, C.F. Brown, R.B.;
Design Automation Conference, 2000. Proceedings 2000. 37th June 5-9, 2000 Page(s):730 - 735
[AbstractPlus](#) | [Full Text: PDF\(716 KB\)](#) | [IEEE CNF](#)
- 21. **Testing a multichip package for a consumer communications application**
Biewenga, A.; Muris, M.; Schuttert, P.; Fawer, U.;
Test Conference, 1998. Proceedings. International 18-23 Oct. 1998 Page(s):222 - 227
Digital Object Identifier 10.1109/TEST.1998.743155
[AbstractPlus](#) | [Full Text: PDF\(604 KB\)](#) | [IEEE CNF](#)
- 22. **A reconfigurable logic machine for fast event-driven simulation**
Bauer, J.; Bershteyn, M.; Kaplan, I.; Vyedin, P.;
Design Automation Conference, 1998. Proceedings 15-19 Jun 1998 Page(s):668 - 671
[AbstractPlus](#) | [Full Text: PDF\(372 KB\)](#) | [IEEE CNF](#)
- 23. **Specification, design and implementation of a digital binary image processor**
O'Rourke, E.; Foley, J.B.;
Applications Specific Integrated Circuits for Digital Signal Processing, IEE Coll 7 Jun 1993 Page(s):8/1 - 8/5
[AbstractPlus](#) | [Full Text: PDF\(248 KB\)](#) | [IEE CNF](#)
- 24. **IEEE standard for VITAL ASIC (application specific integrated circuit) model specification**
IEEE Std 1076.4-2000
2001 Page(s):0_1 - 420
[AbstractPlus](#) | [Full Text: PDF\(1376 KB\)](#) | [IEEE STD](#)

25. **IEEE standard for VITAL Application-Specific Integrated Circuit (ASIC) m specification**
IEEE Std 1076.4-1995
17 May 1996
[AbstractPlus](#) | Full Text: [PDF\(3828 KB\)](#) IEEE STD

Indexed by
 Inspec

[Help](#) [Contact Us](#) [Privacy &](#)
© Copyright 2005 IEEE -